REMARKS

After entry of this response, claims 1-6, 9-17, and 20-35 remain pending. In the present Office Action, claims 28-29 were rejected under 35 U.S.C. § 102(b) as being anticipated by Dearth et al., U.S. Patent No. 5,881,267 ("Dearth"). Claims 1, 9-12, 20-22, and 30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Dearth in view of Feinberg et al., U.S. Patent No. 5,910,903 ("Feinberg"). Claims 2-3, 5-6, 13-14, 16-17, 31-32, and 34-35 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Dearth in view of Feinberg and "Handbook of Simulation" edited by Jerry Banks ("Banks"). Claims 4, 15, and 33 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Dearth in view of Feinberg, Banks, and "CSCI 320 Computer Architecture Handbook on Verilog HDL" by Dr. Daniel C. Hyde ("Hyde"). Claims 23-27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Dearth in view of Hyde. Applicants respectfully traverse these rejections and request reconsideration.

Claims 1-6, 9-17, 20-22, and 30-35

Applicants respectfully submit that each of claims 1-6, 9-17, 20-22, and 30-35 recites a combination of features not taught or suggested in the cited art. For example claim 1 recites a combination of features including: "a hub coupled to the first node and the second node, wherein the hub is configured to route the message packets from the first node to the second node and from the second node to the first node".

The present Office Action alleges that the hub is taught by Dearth's hub 110A and the corresponding description at col. 4, lines 48-57. However, these teachings are: "With each simulated cycle of a clock of bus 214, a hub 110A (FIG. 1) (i) collects data which represents components of the simulated state of bus 204 (FIG. 2) from VBSs 114A (FIG. 1) and 114B, (ii) resolves the current simulated state of bus 214 (FIG. 2), and (iii) sends data representing the resolved state of the simulated bus to VBSs 114A (FIG. 1) and 114B. As a result, VBSs 114A and 114B collectively accurately simulate bus 214 (FIG. 2) which connects circuit parts 212A and 212B which are in turn simulated by DSPs 112A (FIG. 1) and 112B, respectively." (Dearth, col. 4, lines 48-57).

Thus, Dearth teaches a hub that receives data representing the simulated state of the bus in each of the simulation systems, resolves the current state of the bus, and transmits data representing the resolved state to the simulation systems. That is, the data received from one simulation system is not routed to another simulation system. Rather, the received data is operated upon by the hub to create the resolved data. This newly created data is then sent to the hubs. Nothing in this section teaches or suggests "a hub coupled to the first node and the second node, wherein the hub is configured to route the message packets from the first node to the second node and from the second node to the first node".

Furthermore, nothing in Feinberg teaches or suggests the recited hub. As previously noted, Feinberg teaches a control computer that "is overlaid onto the distributed simulation of Fig. 1 without disturbing how the distributed simulation of Fig. 1 operates" (Feinberg, col. 4, lines 26-28). With respect to Fig. 1, Feinberg teaches "The DIS software 110 on each simulation component 100 broadcasts Protocol Data Units ('PDUs') 120 to the DIS software 110 on each of the other simulation components 100. Each PDU 120 comprises information about the particular simulation entity 130 running on the simulation component 100 on which the DIS software 110 is resident so that each simulation component 100 may determine the relationship between each of the simulation entities 130" (Feinberg, col. 1, lines 59-67). Thus, Feinberg's simulation components communicate PDUs directly with each other to perform a distributed simulation. Furthermore, Feinberg's teachings that his invention operates "in the background" (see, e.g., Feinberg, col. 7, lines 13-19) and "without disturbing how the distributed simulation operates" (see, e.g., Feinberg, col. 4, lines 27-28) teaches away from operating the control computer as a hub or inserting a hub.

For at least all of the above stated reasons, Applicants respectfully submit that claim 1 is patentable over the cited art. Claims 2-6 and 9-11, being dependent from claim 1, are similarly patentable over the cited art for at least the above stated reasons. Each of claims 2-6 and 9-11 recite additional combinations of features not taught or suggested in

the cited art. Applicants reserve the right to highlight such additional combinations on appeal.

Claim 12 recites a combination of features including: "communicating at least signal values during the simulating using message packets formatted according to a grammar; and routing the message packets through a hub coupled to the first node and the second node". The teachings of Dearth and Feinberg highlighted above with regard to claim 1 also do not teach the above highlighted features of claim 12. Accordingly, Applicants respectfully submit that claim 12 is patentable over the cited art. Claims 13-17 and 20-22, being dependent from claim 12, are similarly patentable over the cited art for at least the above stated reasons. Each of claims 13-17 and 20-22 recite additional combinations of features not taught or suggested in the cited art. Applicants reserve the right to highlight such additional combinations on appeal.

Claim 30 recites a combination of features including: "the hub is configured to route message packets from the first node to the second node and from the second node to the first node during simulation, the message packets including message packets that communicate at least signal values". The teachings of Dearth and Feinberg highlighted above with regard to claim 1 also do not teach the above highlighted features of claim 30. Accordingly, Applicants respectfully submit that claim 30 is patentable over the cited art. Claims 31-35, being dependent from claim 30, are similarly patentable over the cited art for at least the above stated reasons. Each of claims 31-35 recite additional combinations of features not taught or suggested in the cited art. Applicants reserve the right to highlight such additional combinations on appeal.

Claims 23-27

Applicants respectfully submit that each of claims 23-27 recites a combination of features not taught or suggested in the cited art. For example claim 23 recites a combination of features including: "a first model comprising a representation of logic to perform a non-blocking assignment and logic to schedule a call of at least a first code sequence responsive to the non-blocking assignment, and the first code sequence

comprising instructions executable to sample output signals and drive input signals of a second model".

The Office Action alleges that Hyde teaches the above highlighted features in section 2.7.3, page 15 of 26. While this section of Hyde generally describes blocking and non-blocking assignments in Verilog, including a definition of non-blocking assignments as assignments that evaluate all the right hand sides for the current time unit and assigns the left hands sides at the end of the time unit. However, Applicants respectfully submit that this general description of a non-blocking assignment's functionality does not teach or suggest a model that includes logic to schedule a call to a first code sequence responsive to the non-blocking assignment. Hyde's definition of a non-blocking assignment, when viewed in context, describes the apparent effect of a non-blocking assignment to a human viewing simulation results. For example, Hyde teaches "the effect is that all non-blocking assignments use the old values of variables at the beginning of the current time unit and to assign the registers new values at the end of the current time unit." (Hyde, page 15, section 2.7.3 at the end). However, the Verilog simulator that evaluates the non-blocking assignments need not actually evaluate the right sides at the "beginning" of the time unit, and then later make the assignments at the "end" of the time unit. For example, separate variables could store the original value of a signal and its evaluated value for signals that have non-blocking assignments. Then, the simulator could evaluate the non-blocking assignments at any time without overwriting the old values that might be needed for other non-blocking assignments. Verilog simulators evaluate non-blocking assignments in a variety of fashions (e.g. see Applicants specification page 24, lines 16-20). For example, non-blocking assignment events are typically evaluated as a set at a given point within the order of events. However, nothing in this section requires that a model include logic to schedule a call to a code sequence in response to the non-blocking assignment. The general definition of a non-blocking assignment does not teach or suggest a specific response to a non-blocking assignment.

Furthermore, even if, *arguendo*, Hyde did teach the above model, the combination of Hyde and Dearth still would not teach the combination of features in claim 23. While

Dearth teaches a DSP 112 and a VBS 114 that simulate a bus in a simulation system, these two components are HDL models that are evaluated by a simulator. Thus, neither of these models is a first code sequence, a call to which is scheduled in response to a non-blocking assignment in the other model, that samples and drives signals in a second model.

For at least the above stated reasons, Applicants submit that claim 23 is patentable over the cited art. Claims 24-27 depend from claim 23, and thus are patentable over the cited art for at least the above stated reasons as well. Each of claims 24-27 recite additional combinations of features not taught or suggested in the cited art. Applicants reserve the right to highlight such additional combinations on appeal.

Claims 28-29

Applicants respectfully submit that each of claims 28-29 recites a combination of features not taught or suggested in the cited art. For example claim 28 recites a combination of features including: "count timesteps in a distributed simulation system; and cause a cycle-based simulator to evaluate a clock cycle in a model responsive to a number of the timesteps equaling a number of timesteps per clock cycle of a clock corresponding to the model".

The Office Action alleges that Dearth teaches the above highlighted features at col. 10, lines 31-44. However, these teachings are: "In step 610, VBS 114A (FIG. 5) delays for a period of simulated time indicated by data stored in post delay field 510. Simulated time is kept by simulation system 116A (FIG. 1) and represents time elapsing during operation of the circuit simulated by simulation system 116A. FIG. 7 shows simulated signals A, B, and CLOCK of bus 214 (FIG. 2). After a delay 712 (FIG. 7) after rising edge 710 of simulated clock signal CLOCK, i.e., at resolve time 702A, posting by VBS 114A (FIG. 4) is initiated. By delaying a period of time *from the rising edge* of the clock signal represented by clock field 504 (FIG. 5), the state of bus 214 (FIG. 2) is resolved at a simulated time at which bus 214 should have a steady state." Thus, Dearth teaches delaying a period of time from the rising edge of the clock signal in the system to

reach at time at which the bus 214 should be stable. This amount of time is not a full clock cycle of the clock signal. Rather, it is some specified delay from the rising edge (the post delay) that is less than a clock cycle. Accordingly, this section of Dearth cannot teach or suggest causing a cycle-based simulator to evaluate a clock cycle responsive to a number of the timesteps equaling a number of timesteps *per clock cycle* of the clock corresponding to the model. If Dearth were to operate in this fashion, Dearth would delay until the next rising edge of the simulated clock signal, and would not accurately simulate the model.

Furthermore, the Office Action alleges that "delaying the simulation clock signal represented by clock 504 is inherently a delay equal to a number of timesteps per clock cycle of the clock corresponding to the model." Applicants respectfully disagree. First, Dearth does not teach delaying a simulation clock signal. Instead, Dearth teaches delaying from the rising edge of the simulation clock signal before posting signals to the resolver in the hub". This delay is the amount of time from the rising edge before signals stabilize, and clearly cannot be equal to the number of timesteps in the clock cycle defined by the clock signal. As shown in Fig. 7, the delay is some small portion of the clock cycle, not a full clock cycle.

The Office Action further reasons that the only way that Dearth's simulator to perform a delay is to count a number of timesteps equal to the desired delay. Since the desired delay is not a clock cycle, but some small period of time from the rising edge of the clock cycle, this reasoning still does not support the proposition that Dearth anticipates "count timesteps in a distributed simulation system; and cause a cycle-based simulator to evaluate a clock cycle in a model responsive to a number of the timesteps equaling a number of timesteps per clock cycle of a clock corresponding to the model".

Still further, Applicants submit that Dearth does not teach a cycle-based simulator. Rather, Dearth teaches that after posting signals, a small amount of simulation time elapses to allow any effects on the state of the bus to dissipate (col. 11, lines 2-4), then proceeds to reap the bus state from the resolver and drives the lines on the bus (col.

11, lines 20-35). All of this occurs during the same simulated clock cycle. Accordingly, Dearth is describing event-based simulation, not cycle-based simulation.

For at least the above stated reasons, Applicants submit that claim 28 is patentable over the cited art. Claim 29 depends from claim 28, and thus is patentable over the cited art for at least the above stated reasons as well. Claim 28 recites additional combinations of features not taught or suggested in the cited art.

CONCLUSION

Applicants submit that the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5181-96200/LJM.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☐ Petition for Extension of Time

☐ Request for Approval of Drawing Changes

☐ Notice of Change of Address

☐ Please debit the above deposit account in the amount of $ for fees ( ).

☒ Other: Information Disclosure Statement and copy of Office Action from 10/008,155

Respectfully submitted,

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